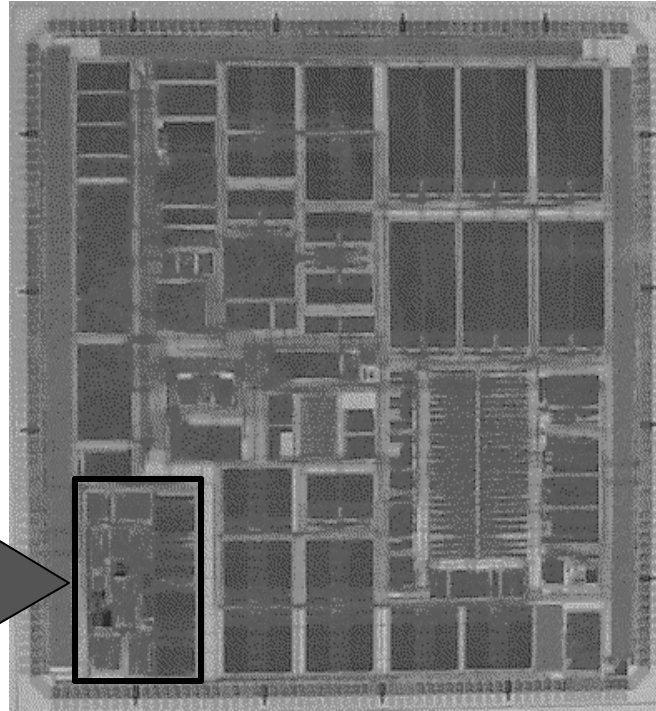


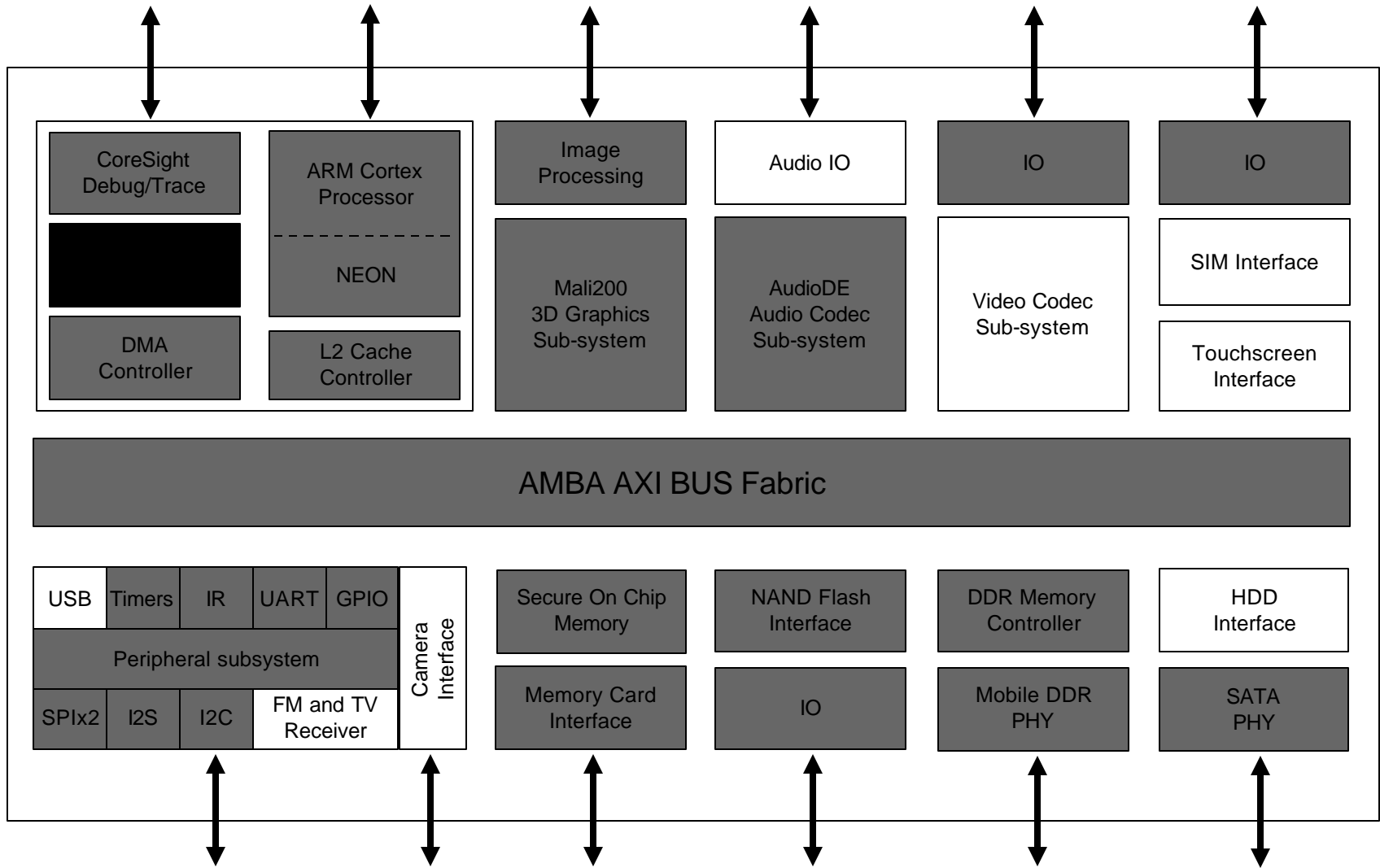
Embedded Processors in SoC Design

Embedded microprocessors

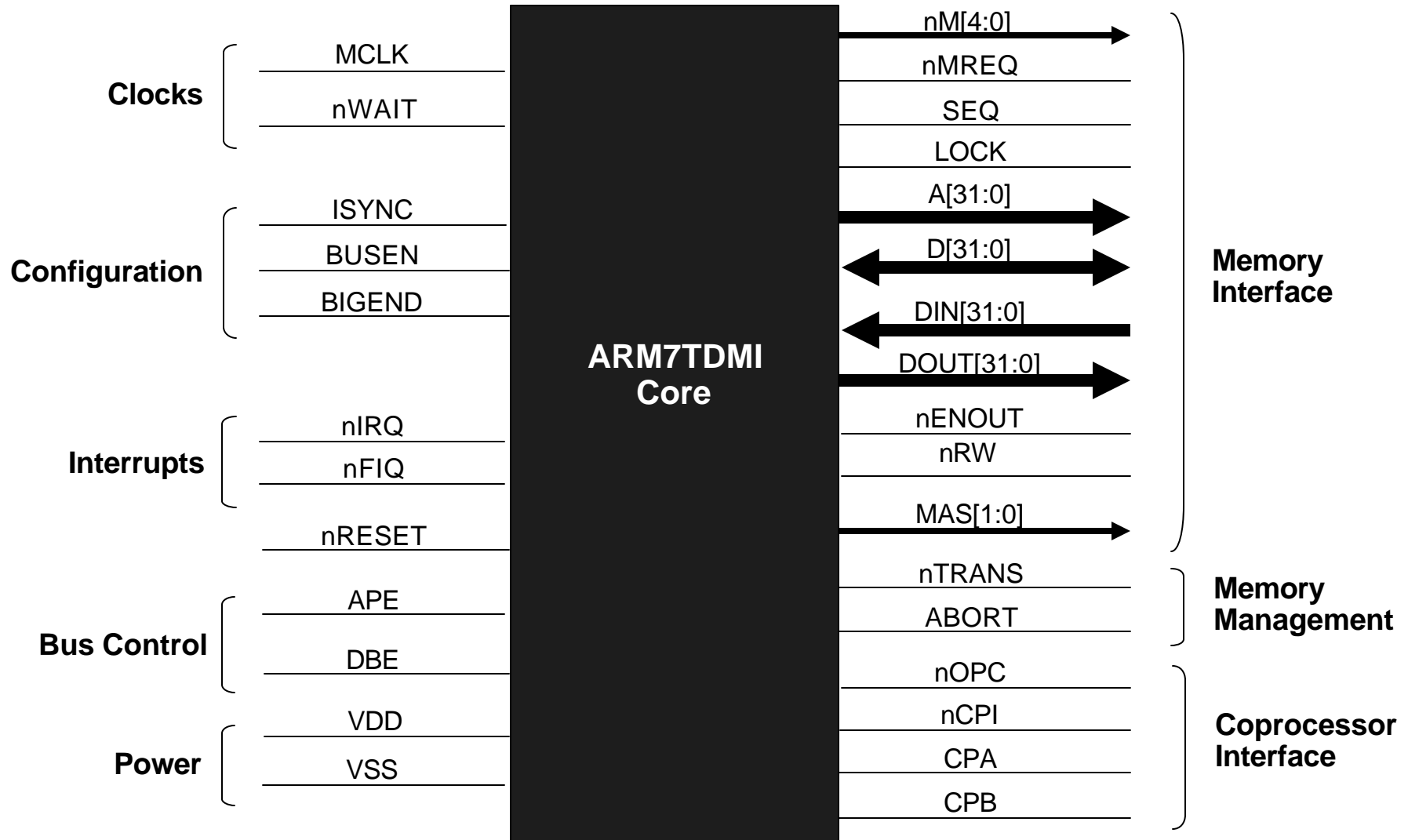
ARM7TDMI



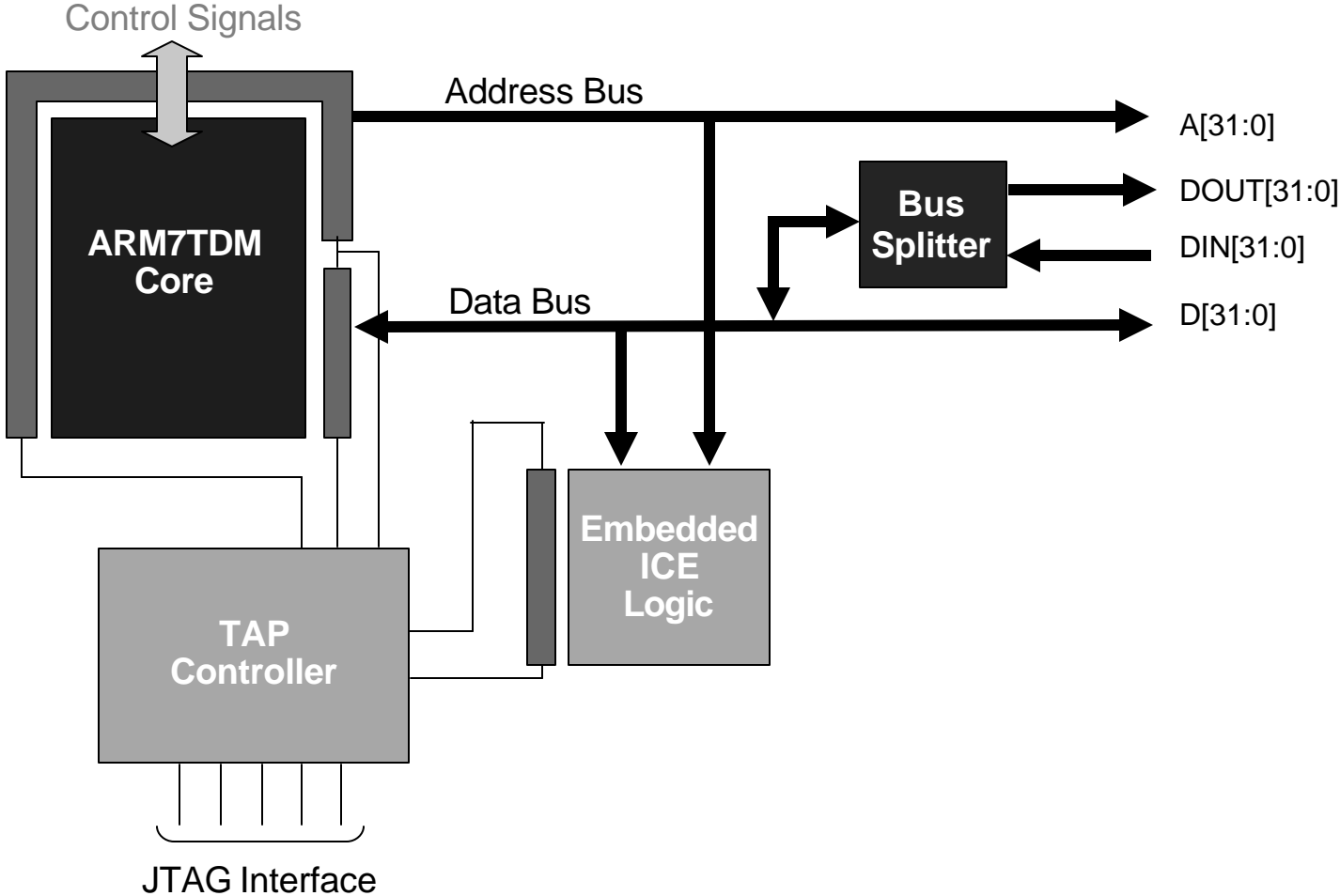
Example: Connected Mobile Computer



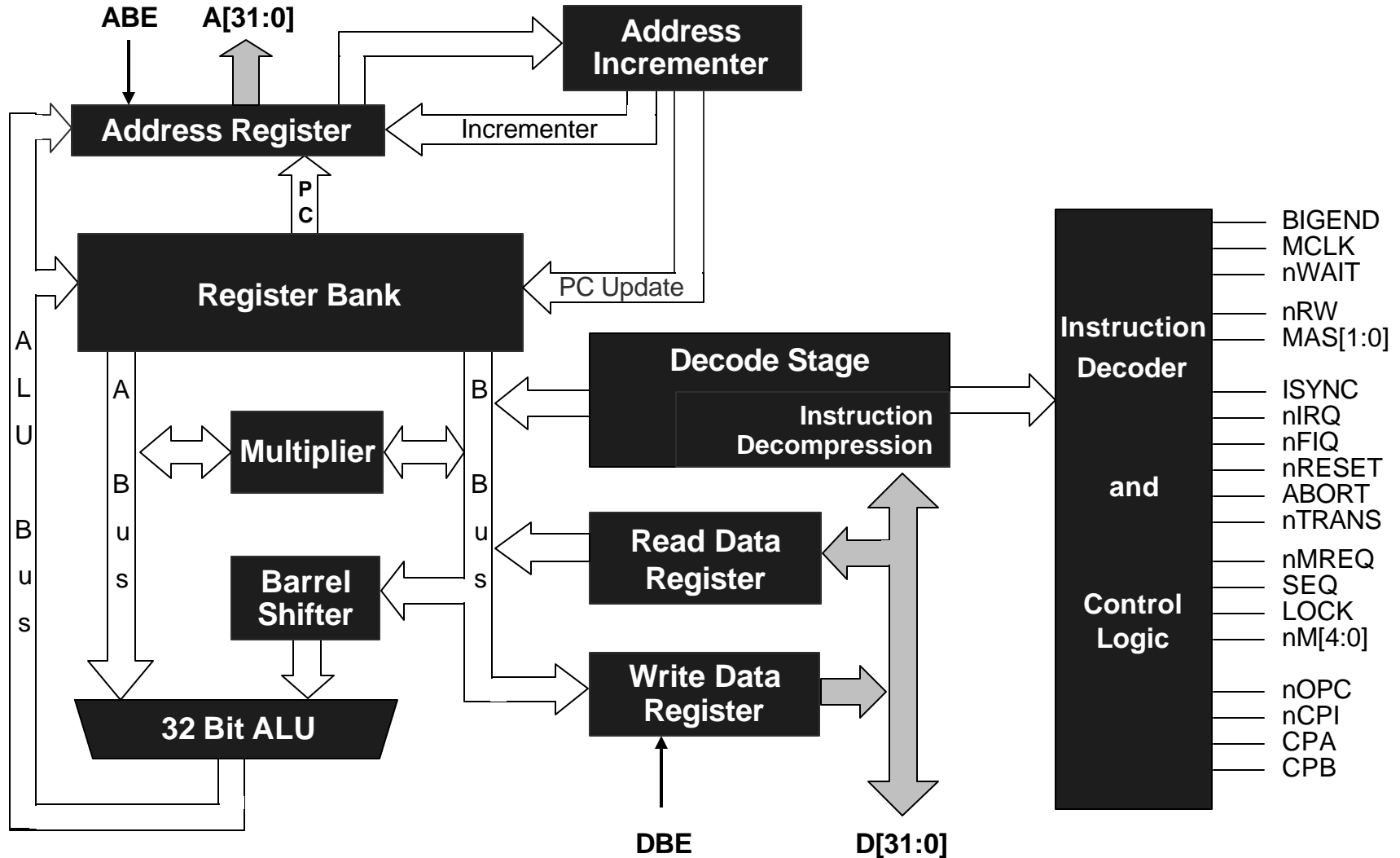
ARM7TDMI Core Signals



ARM7TDMI Block Diagram



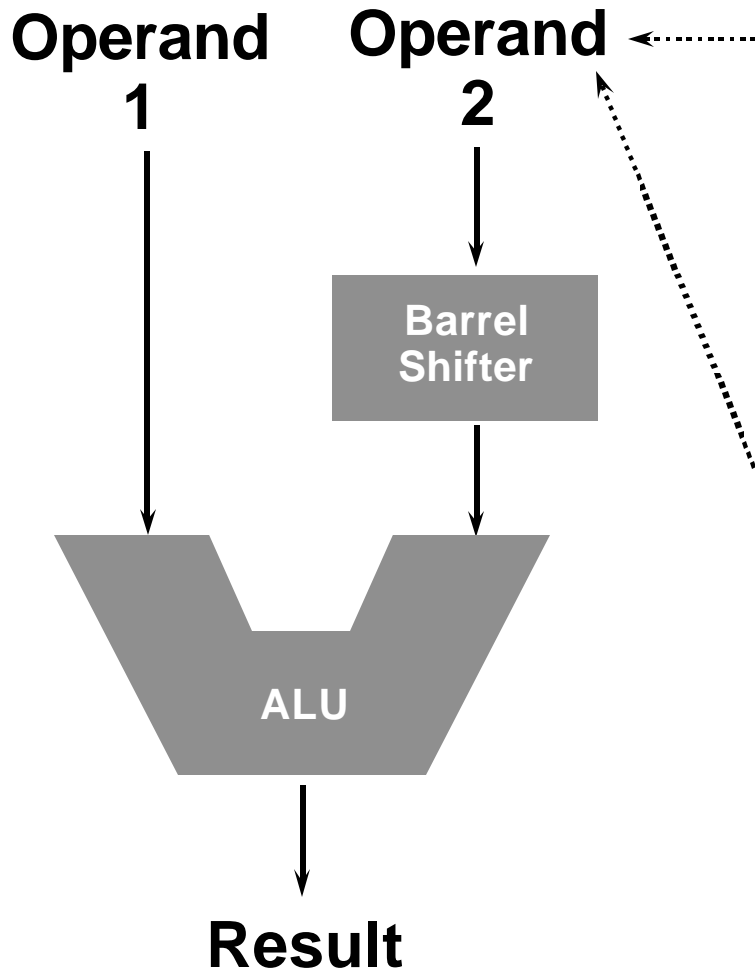
The ARM7TDM Core



Data processing Instructions

- Consist of :
 - Arithmetic: **ADD ADC SUB SBC RSB RSC**
 - Logical: **AND ORR EOR BIC**
 - Comparisons: **CMP CMN TST TEQ**
 - Data movement: **MOV MVN**
- These instructions only work on registers, NOT memory.
- Syntax:
<Operation>{<cond>}{S} Rd, Rn, Operand2
 - Comparisons set flags only - they do not specify Rd
 - Data movement does not specify Rn
- Second operand is sent to the ALU via barrel shifter.

Using the Barrel Shifter



Register, optionally with shift operation

- Shift value can be either be:
 - 5 bit unsigned integer
 - Specified in bottom byte of another register.
- Used for multiplication by constant

Immediate value

- 8 bit number, with a range of 0-255.
 - Rotated right through even number of positions
- Allows increased range of 32-bit constants to be loaded directly into registers

Single register data transfer

LDR STR Word

LDRB STRB Byte

LDRH STRH Halfword

LDRSB Signed byte load

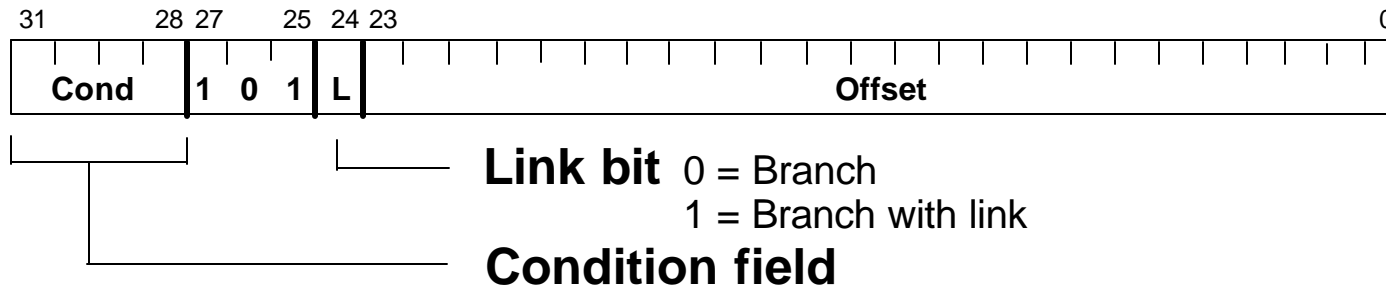
LDRSH Signed halfword load

- Memory system must support all access sizes
- Syntax:
 - LDR{<cond>}{<size>} Rd, <address>
 - STR{<cond>}{<size>} Rd, <address>

e.g. LDREQB

Branch instructions

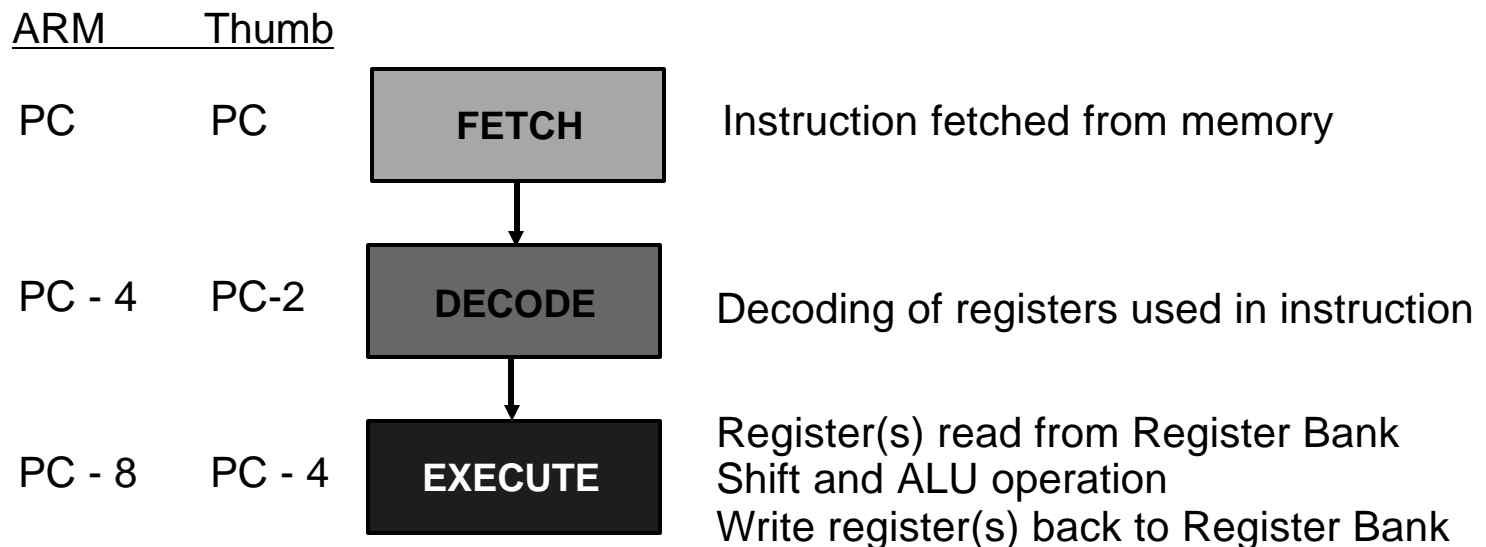
- Branch : `B{<cond>} label`
- Branch with Link : `BL{<cond>} subroutine_label`



- The processor core shifts the offset field left by 2 positions, sign-extends it and adds it to the PC
 - ± 32 Mbyte range
 - How to perform longer branches?

The Instruction Pipeline

- The ARM7 family uses a 3 stage pipeline in order to increase the speed of the flow of instructions to the processor.
 - Allows several operations to be undertaken simultaneously, rather than serially.



- The PC points to the instruction being fetched, not the instruction being executed.

Optimal Pipelining

Cycle		1	2	3	4	5	6
<u>Operation</u>							
ADD	Fetch	Decode	Execute				
SUB		Fetch	Decode	Execute			
MOV			Fetch	Decode	Execute		
AND				Fetch	Decode	Execute	
ORR					Fetch	Decode	Execute
EOR						Fetch	Decode
CMP							Fetch
RSB							

- In this example it takes 6 clock cycles to execute 6 instructions
- All operations here are on registers (single cycle execution)
- Clock cycles per Instruction (CPI) = 1

LDR Pipeline Example

Cycle	1	2	3	4	5	6		
<u>Operation</u>								
ADD	Fetch	Decode	Execute					
SUB		Fetch	Decode	Execute				
LDR			Fetch	Decode	Execute	Data	Writeback	
MOV				Fetch	Decode			Execute
AND					Fetch			Decode
ORR								Fetch

- In this example it takes 6 clock cycles to execute 4 instructions
- Clock cycles per Instruction (CPI) = 1.5

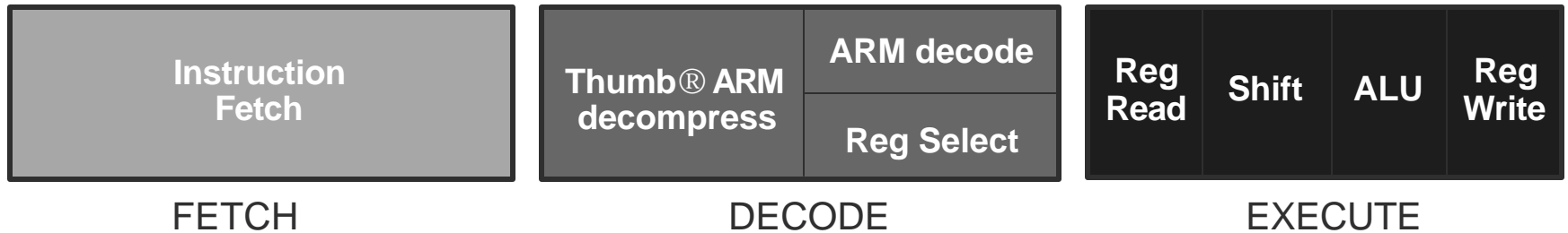
Branch Pipeline Example

Cycle		1	2	3	4	5		
<u>Address</u>	<u>Operation</u>							
0x8000	BL	Fetch	Decode	Execute	Linkret	Adjust		
0x8004	X		Fetch	Decode				
0x8008	XX			Fetch				
0x8FEC	ADD				Fetch	Decode	Execute	
0x8FF0	SUB					Fetch	Decode	Execute
0x8FF4	MOV						Fetch	Decode
								Fetch

- Breaking the pipeline
- Note that the core is executing in ARM state

Pipeline changes for ARM9TDMI

ARM7TDMI



ARM9TDMI



Longer Pipelining

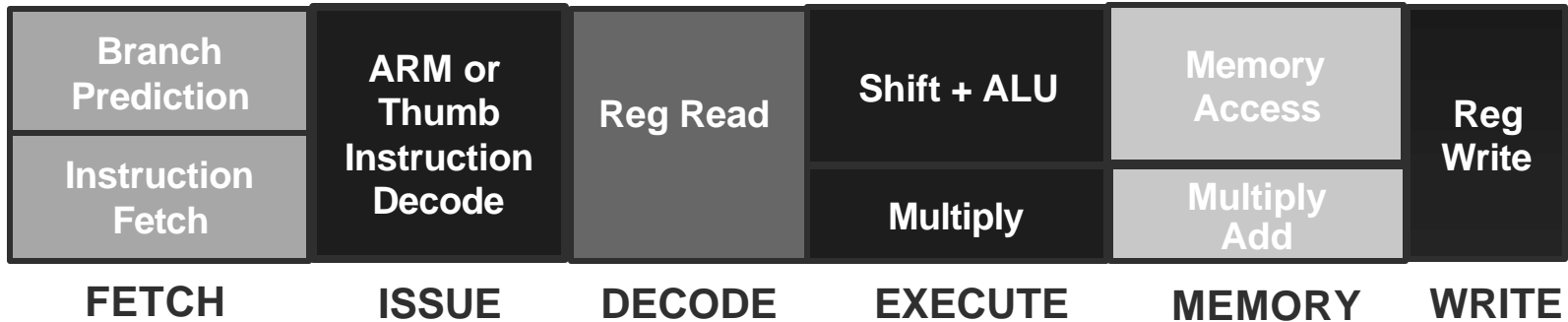
Cycle		1	2	3	4	5	6	7	8	9	
Operation											
ADD	R1, R1, R2	F	D	E	I	W					
SUB	R3, R4, R1		F	D	E	I	W				
LDR	R4, [R7]			F	D	E	M	W			
AND	R6, R3, R1				F	D	E	I	W		
ORR	R8, R3, R4					F	D	E	I	W	
EOR	R3, R1, R2						F	D	E	I	W

F - Fetch D - Decode E - Execute I - Interlock M - Memory
 W - Writeback

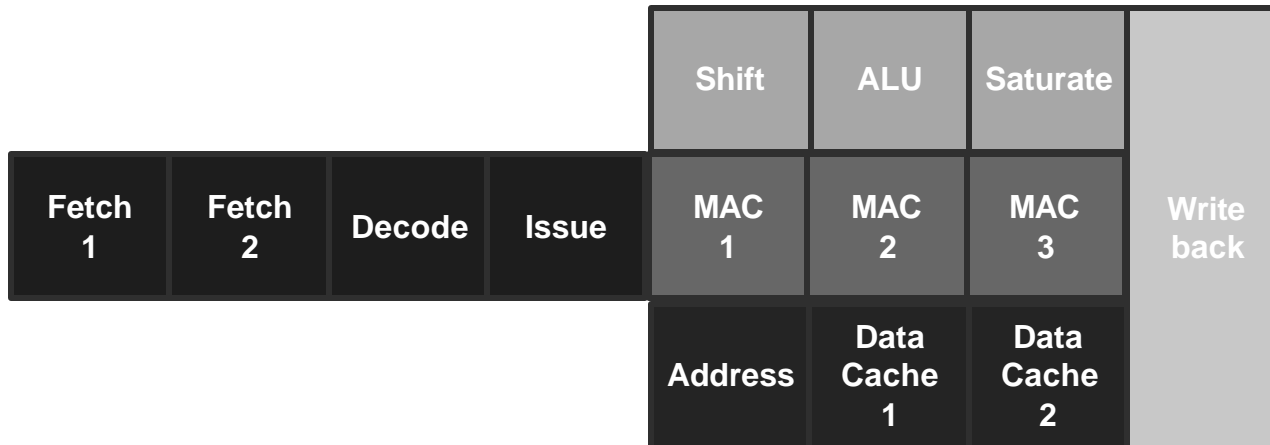
- In this example it takes 6 cycles to execute 6 instructions, CPI of 1.
- The LDR instruction does not cause the pipeline to interlock

ARM10 vs. ARM11 Pipelines

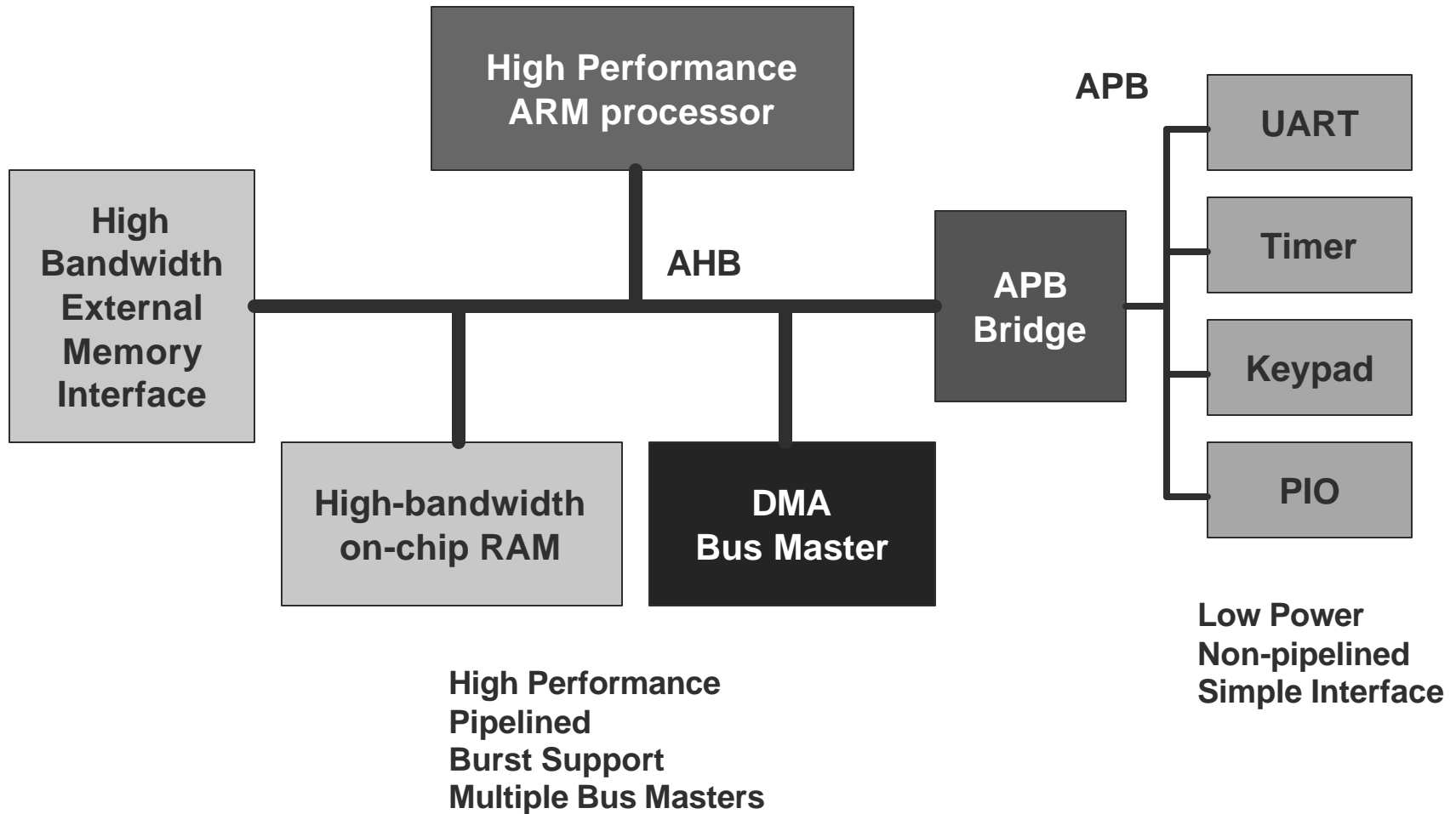
ARM10



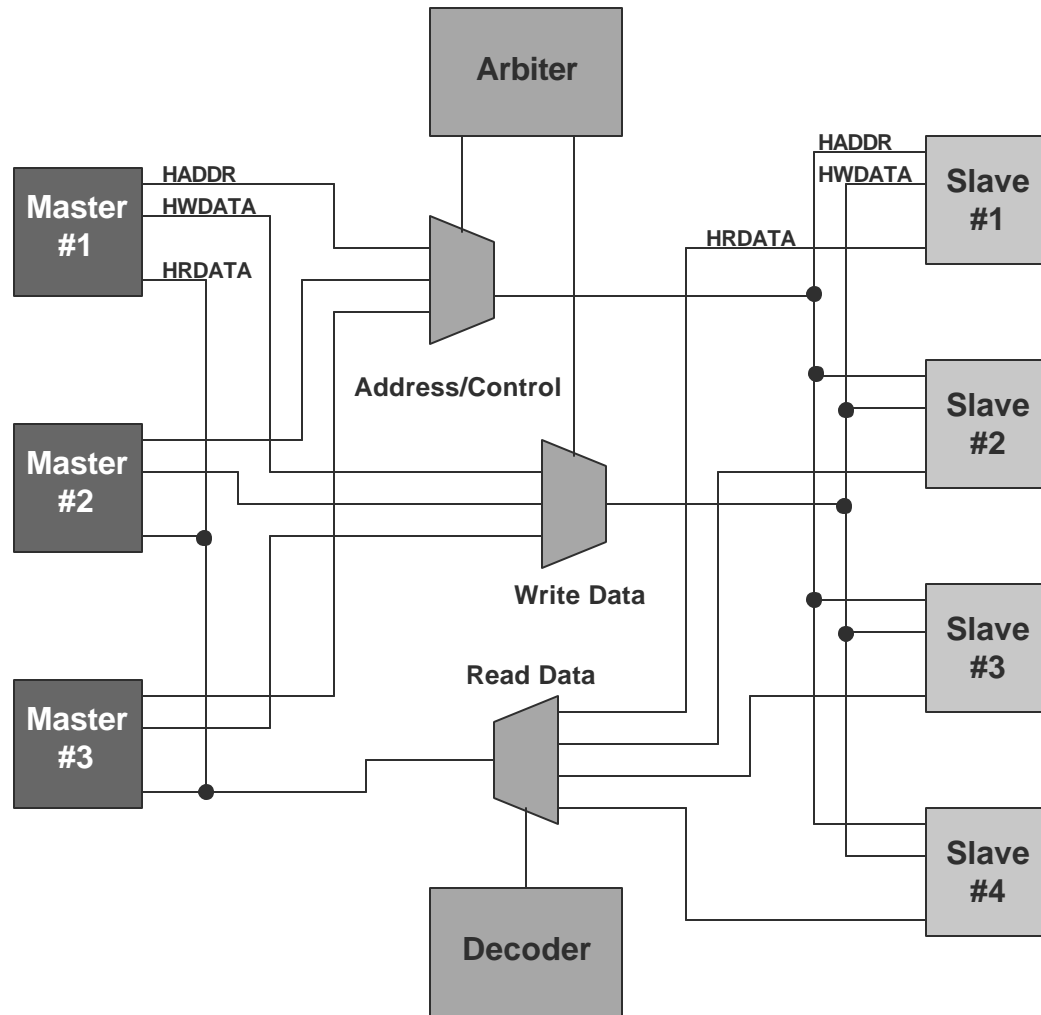
ARM11



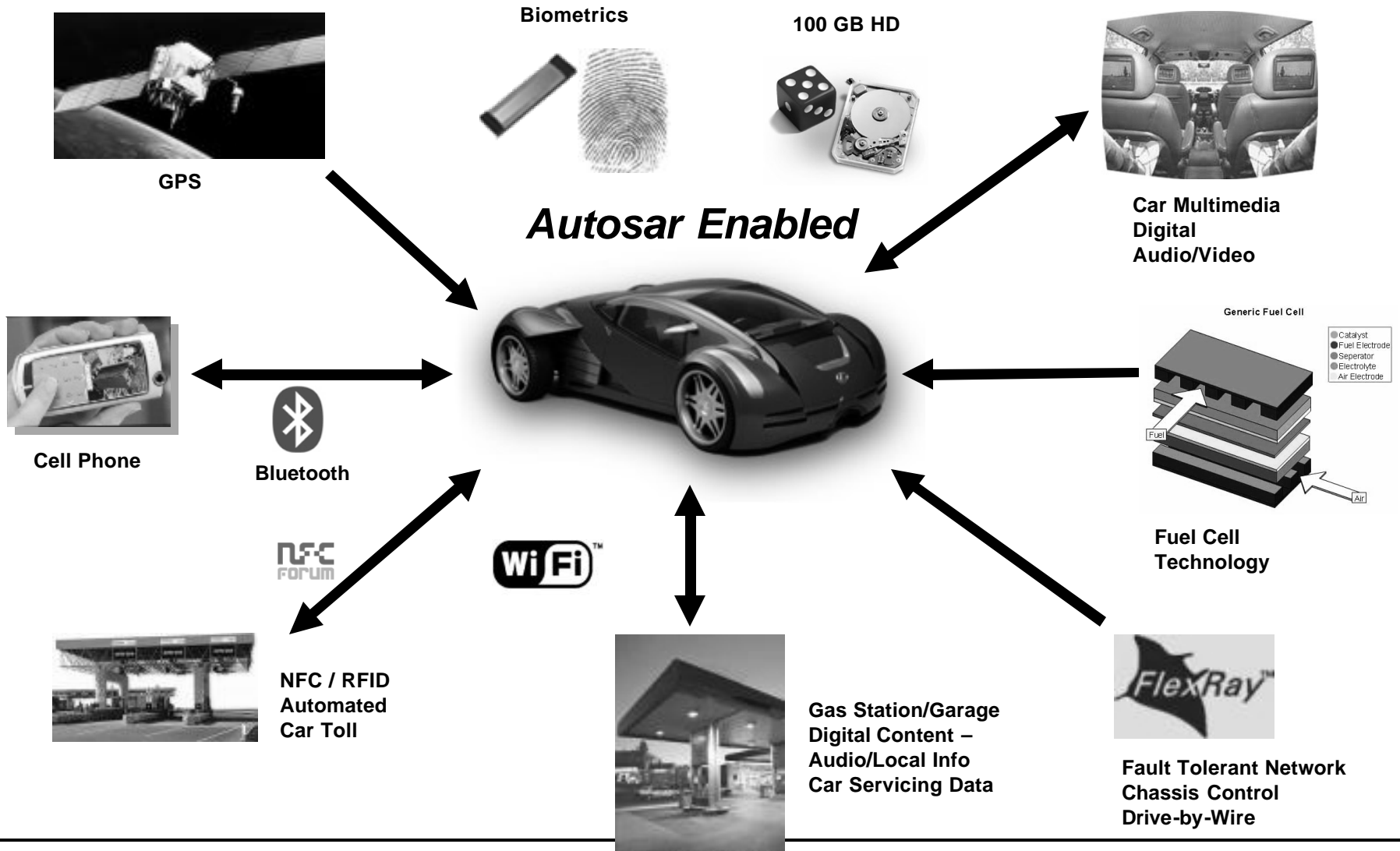
An Example AMBA System



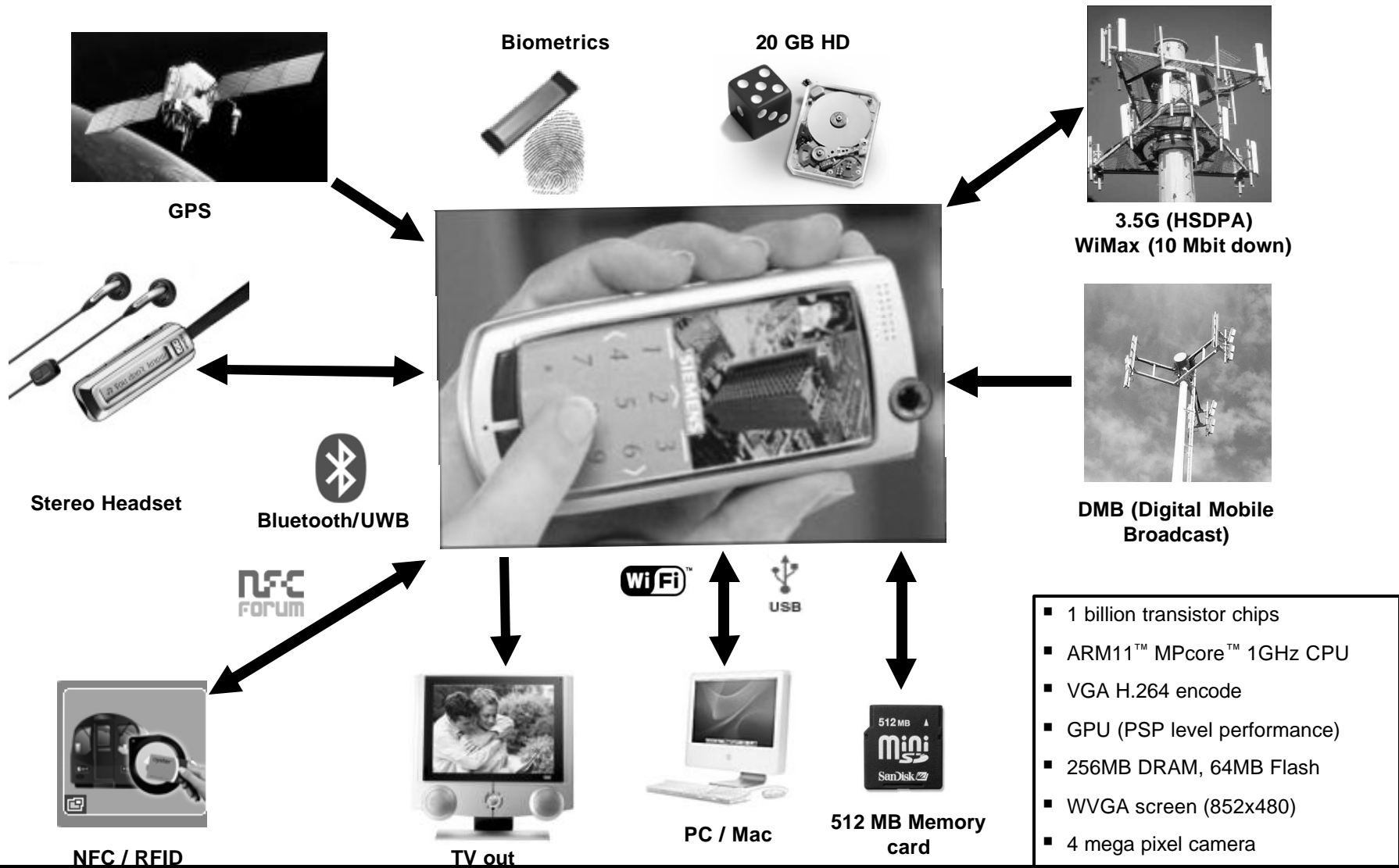
AHB Structure



High-End Car of 2012



Concept Smart Phone of 2008



- 1 billion transistor chips
- ARM11™ MPcore™ 1GHz CPU
- VGA H.264 encode
- GPU (PSP level performance)
- 256MB DRAM, 64MB Flash
- WVGA screen (852x480)
- 4 mega pixel camera

**Questions or comments:
university@arm.com**