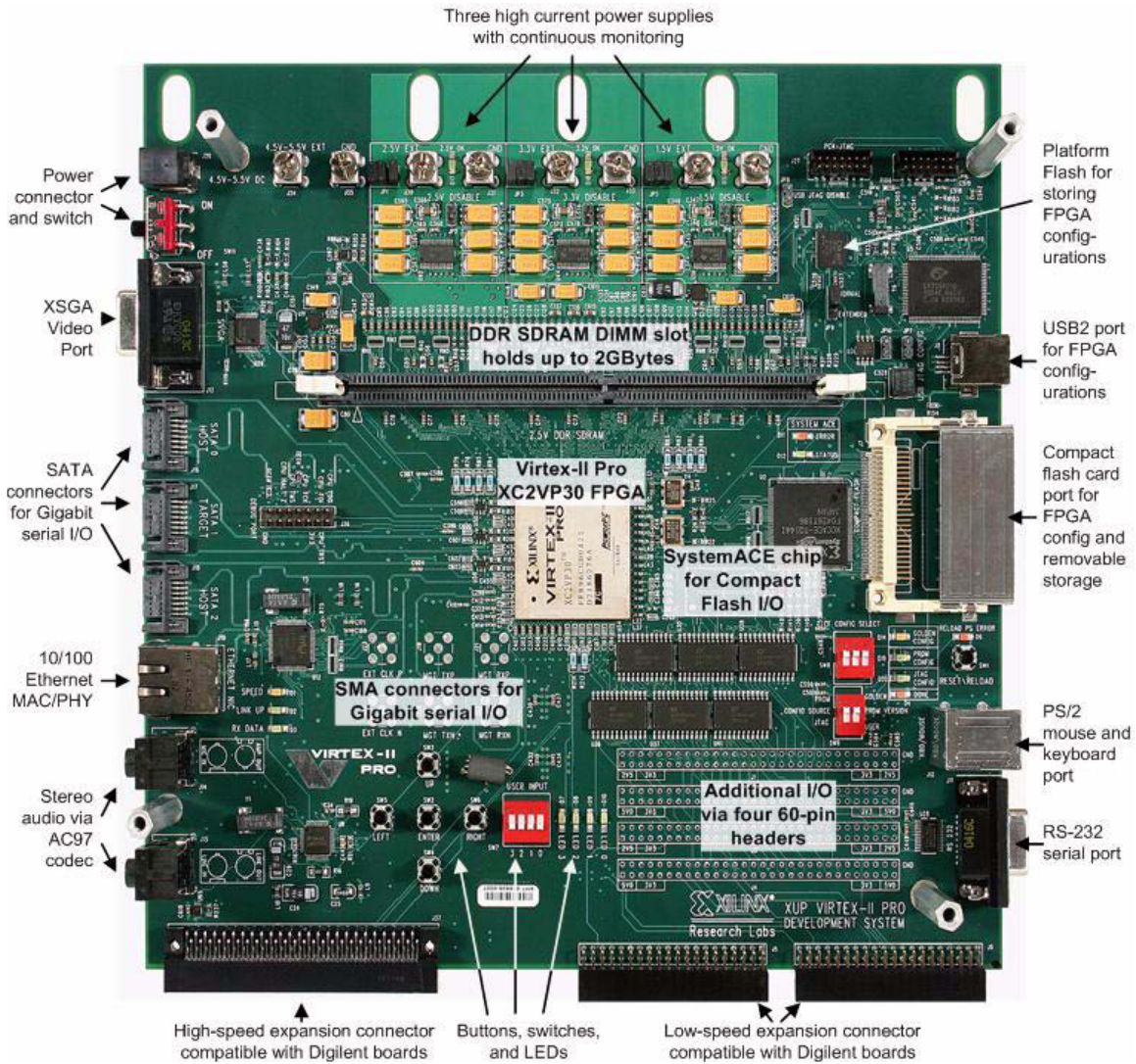


ECEN 449 – MICROPROCESSOR SYSTEM DESIGN

Department of Electrical & Computer Engineering
Texas A&M University



Xilinx Virtex II Pro Development Board

The XUP Virtex-II Pro development system consists of a high performance Virtex-II Pro FPGA surrounded by a collection of peripheral components that can be used to create a complex system.

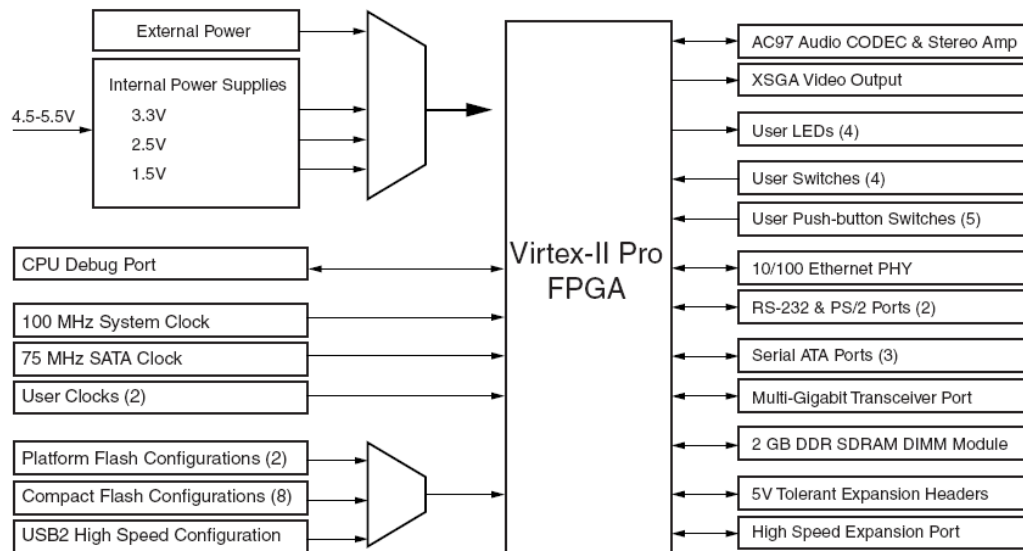


Figure 2. Block Diagram

We shall be interfacing some of these peripheral components in this lab course. For an overview of each of the components in the block diagram of Figure 2, please refer to the [XUPV2P User guide.pdf](#).

The Virtex-II Pro board is a programmable FPGA, with two integrated Power PC processors on the chip. So, it allows us to do projects in hardware alone (using the FPGA) or software (using the PowerPC processor) or both.

We shall be using the following software tools to program the FPGA:

1. Integrated Software Environment (ISE)
 - ISE enables you to start design using HDL (VHDL, Verilog HDL, ABEL), Schematic design files, state machines, etc.
 - We shall be using Verilog HDL for our labs.
2. Xilinx Platform Studio (XPS)
 - It is a tool which can be used for creating and editing both software and hardware.
 - It supports both the PowerPC hard processor core and the MicroBlaze soft processor core designs. Further details of the same would be provided in the lab using XPS.

The labs you will work on are as follows:

S.No.	Duration (# Weeks)	Title	Editorial Comments
1	1	Using the Integrated Software Environment (ISE)	<ul style="list-style-type: none"> - Use ISE to light up the LEDs based on the status of the DIP Switches. - This experiment will be performed by writing Verilog code which will run on the FPGA hardware.
2	2	Interfacing LEDs and Switches using XPS	<ul style="list-style-type: none"> - This experiment involves controlling the LEDs using software, using the XPS tool. - The software (C code) runs on the PowerPC microprocessor on the XUP board.
3	1	Adding Custom IP using XPS	<ul style="list-style-type: none"> - This experiment involves using both the FPGA (hardware) and PowerPC (software) in tandem. - A Custom IP (Verilog code) is used to implement a multiplier. The Verilog code reads the value from two registers (say R1 and R2) and writes the multiplied output to a third register (R3). - Software is used for testing the multiplier. The software code should write values to registers R1 and R2 and read the multiplication result from R3, and display the values of R1, R2 and R3 on a hyperterminal screen.

Please make sure that you save your working program after each lab. Program created in one lab may be used in the subsequent labs.