ECEN 449: Microprocessor System Design
Department of Electrical and Computer Engineering
Texas A&M University

Assignment #4

Solutions

1. A 32 GB flash drive is organized as follows:

   - It can be accessed in 512-byte sectors
   - It contains 2048 banks.

   If the drive is accessed with a 40-bit address by a processor employing byte-level addressing, show how the address bits are used in accessing data from the flash drive.

   Solution. Lets us say that the address bits are a_{39}, a_{38}, a_{37}, ... a_2, a_1, a_0. To address 32GB we need only 35-bits. Therefore, address bits a_{39}, a_{38}, a_{37} a_{36} and a_{35} are not used. Bits a_0 to a_8 are used to access 1 byte from 512-byte sector. We would like to read from all the banks at the same time therefore, we use bits a_9 to a_{20} to access different banks. Rest of the bits a_{21} to a_{34} are used to access different memory location inside a bank. □

2. A memory is organized as an interleaved memory with 8 banks (also known as 8-way interleaving) and each memory bank contains a block of 64 bits (or 2 32-bit words). If a matrix A (64x64) is stored in this memory,

   (a) What is the fastest time to access all of the data in the matrix?

   (b) What is the slowest time to access all of the data in the matrix?

   Each element of the matrix is 32 bits (1 word). You can assume that data is stored in a row-major fashion.

Solution. Let the matrix A is stored in interleaved memory in row major order as shown in Figure 1. Also let the time required to access one element from memory bank is K ns. Note that the maximum number of outstanding request at the memory is 16.

(a) The fastest way to access all of the data of A is to access the elements of A in row major order. For this, 16-elements of the matrix A are accessed together in row major order. For example $a_{0,0}$, $a_{0,1}$, ... $a_{0,15}$ are accessed in one request and then the elements $a_{0,16}$, $a_{0,17}$, ... $a_{0,31}$ are accessed and so on. In this way, the time required to access all elements of A is $4 \times 64 \times K$ ns.

(b) The slowest way is to access the elements of A in column major order. In this case, all 16 outstanding memory request elements are in the same bank. Therefore, only one element can be accessed in K ns. Thus, the time required to access all elements of A is $64 \times 64 \times K$ ns.

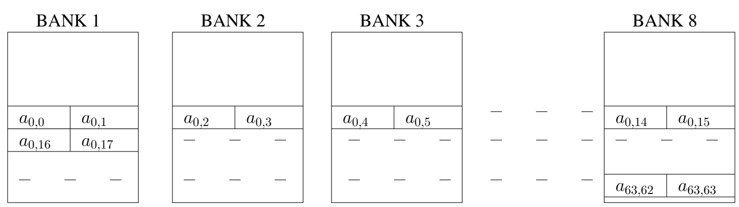

Figure 1: Memory Bank

□

3. Consider a wire on a printed circuit board (PCB). The board is made out of FR4 material (κ = 4.2). Assume that the characteristic impedance of the board is 50 Ω. The length of the wire is 0.1m. Suppose the driver (source) resistance is 10 Ω, and the termination resistor (at the end of the wire) is 200 Ω. The driver voltage changes from 0V to 5V at time $t = 0$.

   (a) What is the velocity of wave propagation in a wire on the PCB? The speed of light is $c = 3 \times 10^8$ m/s.

   (b) What is the inductance per unit length of the wire?

   (c) What is the capacitance per unit length of the wire?

   (d) What is the voltage at the receiving end of the wire, at time $t = \infty$?

   (e) Draw the waveform of the signal at the receiving end of the wire, up to time $t = 13t_d$.

Solution. (a) The velocity (v) of wave propagation is:
$v = \frac{c}{\sqrt{\kappa}} = 1.4638 \times 10^8$ m/s

(b) Let Z_o is the characteristic impedance of the board. The inductance (L) per unit length of the wire is:
$L = \frac{Z_o}{v} = 34.15 \times 10^{-8}$ H

(c) The capacitance (C) per unit length of the wire is:
$C = \frac{1}{vZ_o} = 1.366 \times 10^{-10}$F

(d) The voltage at the receiving end of the wire, at time $t = \infty$ is:
$V_{t=\infty} = 5\frac{200}{200+10} = 4.762V$.

(e) The waveform of the signal at the receiving end of the wire is shown in Figure 2.

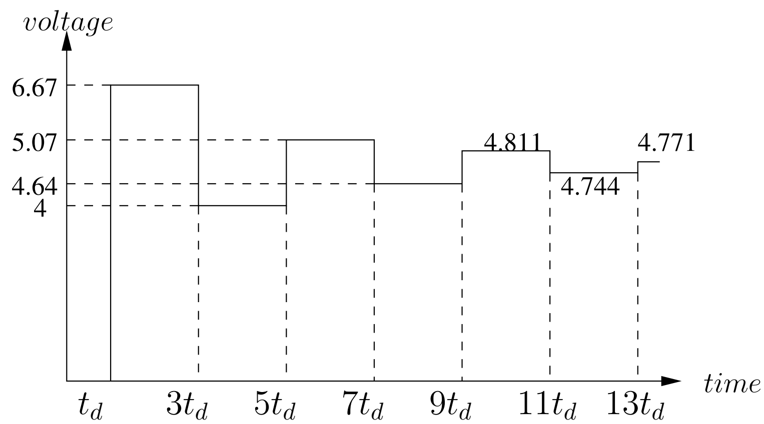

Figure 2: Votlage waveform at receiver's end

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