

ECEN 449: Microprocessor System Design
Department of Electrical and Computer Engineering
Texas A&M University

Assignment #1

Due Friday, September 14, 2007

1. [15 points.]

Suppose we have the following three designs to implement. Which style (among the choice of custom hardware, ASIC, reconfigurable hardware or software) will be the best style for each design? Assume that the reconfigurable hardware can run at up to 500MHz, while the ASIC can run at 1.5GHz, and the custom hardware can run at up to 4GHz.

- (a) Design 1 involves a lookup table for an internet protocol (IP) router application. The functionality of this design is that it looks up IP addresses (32 bits) and returns the router interface (4 bits) for this address. Data is fed to this design serially at 1Gbit/second. Design 1 will be used by Cisco, which expects to sell it in high volumes since it will be used in routers for home use. This product must be developed within 9 months.
- (b) Design 2 also involves a lookup table for an internet protocol (IP) router application. But the difference is that this design will be used in the internet backbone, for routing IP traffic between cities, and will be sold in low volumes. The functionality of this design is that it looks up IP addresses (32 bits) and returns the router interface (12 bits) for this address. Data is fed to this design serially at 10 Gbit/second. This product must be developed within 6 months.
- (c) Design 3 is an automotive engine controller, which will be sold to GM and Toyota for all their cars. It coordinates all engine functionality, and must operate at a clock frequency of 2GHz. It must be developed in 4 years, for the automobiles developed for model years 2011 through 2020.

2. [15 points.]

Consider the Verilog code fragment below:

```

`define BUS_SIZE 64; \\leading char is a backtick
module MYMODULE (A, b, C, d)
input a, B;
output C, d;
wire L1 L2 L3(1:4);
reg [3:4] BUS[1:16];
reg [4:3] NEWBUS[16:1];
integer X, Y;
wor #ARBITRATION_bit, \#Acknowledge_bit;
wand [0:15] VECTOR_SEQUENCE[0:15]; //16 bit vector sequence of width 16
`define BUS_SIZE 32; \\leading char is a backtick
\\ this ends all declarations
\\ for my module
/* Now the statements begin */

L3 = (3 * 2)' HF;
A = 1;
b = 0;
endmodule;

```

Indicate and fix all the syntactical errors in this code.

3. [20 points.]

Write a Verilog module (behavioral) to implement a electronic thermometer. It receives an real numbered input voltage V such that $V = 0.025 \times T$, where T is the temperature in Celsius. The temperature range should be checked to be between 0 and 100 degrees Celsius (both values inclusive). If this range check fails, an output MINUSINFINITY should be driven (if the temperature is below 0 degrees Celsius), or the output PLUSINFINITY should be driven (if it is above 100 degrees Celsius). The design should sample the temperature value whenever there is an event on CLOCK (an input signal). When there is an event on PRINT (another input signal) the Fahrenheit value of the temperature is calculated and written to the output RESULT (which is a binary number of appropriate length). For example, if the temperature is 15 degrees Farenheit, and if the length of RESULT was determined by you to be 5 bits, then the RESULT value would be 01111. Whenever the range check fails, RESULT is assigned all 1's.

Provide comments in your code.