A 2.8-mW Sub-2-dB Noise-Figure Inductorless Wideband CMOS LNA Employing Multiple Feedback

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Abstract—A wideband low-noise amplifier (LNA), which is a key block in the design of broadband receivers for multiband wireless communication standards, is presented in this paper. The LNA is a fully differential common-gate structure. It uses multiple feedback paths, which add degrees of freedom in the choice of the LNA transconductance to reduce the noise figure (NF) and increase the amplification. The proposed LNA avoids the use of bulky inductors that leads to area and cost saving. A prototype is implemented in IBM 90-nm CMOS technology. It covers the frequency range of 100 MHz to 1.77 GHz. The core consumes 2.8 mW from a 2-V supply occupying an area of 0.03 mm$^2$. Measurements show a gain of 23 dB with a 3-dB bandwidth of 1.76 GHz. The minimum NF is 1.85 dB, while the average NF is 2 dB across the whole band. The LNA achieves a return loss greater than 10 dB across the entire band and a third-order input intercept point (IIP$_3$) of $-2.85$ dBm at the maximum gain frequency.

Index Terms—Common gate (CG), feedback, inductorless, low-noise amplifier (LNA), low power, noise figure (NF), wideband LNA.

I. INTRODUCTION

MULTIBAND multistandard concepts have gained considerable interest in modern wireless communications systems [1]–[4]. To support a wide set of communication standards and to accommodate different applications in a single device, broadband transceivers are essential and inevitably in demand. A wideband RF receiver front-end architecture constructed by one single path [5] provides lower cost, area, and power consumption compared to the parallel-path architectures [6], [7]. The single-path wideband concept can also accommodate emerging standards for cognitive radio applications, resulting in efficiency improvement in utilizing scarce spectrum resources.

One of the major challenges in wideband receivers is the design of a wideband low-noise amplifier (LNA) that is shared among different standards. As the first block in the receiver chain, such an LNA should achieve good impedance matching, high and flat gain, and low noise figure (NF) across a wide frequency band. In addition, good linearity and low area and power consumption LNAs are required for high-performance and low-cost radios.

Recently, many wideband LNAs in CMOS technology have been reported, including distributed amplifiers [8] and resistive shunt feedback amplifiers [9], [10]. The former offers superior bandwidth in terms of high power consumption, large area, and deterioration of noise performance, which limits its widespread applications. The latter provides good broadband matching, noise, and gain, but it is hampered by greater power consumption, which makes them unattractive for low-power applications. Other implementations are inductor-based, such as L-degenerated broadband LNAs [11]. They have good performance in terms of NF and power consumption. However, the use of area consuming on-chip bulky inductors makes them unattractive for use in upcoming wireless low-cost transceivers.

One of the wideband LNA topologies that has been widely investigated is the common-gate low-noise amplifier (CGLNA). The CGLNA is attractive compared to other topologies as it features wideband input impedance matching. Also, it offers good linearity, stability, and low power consumption. However, its main drawback is the relatively high NF [12]. This is due to the input matching condition, which restricts a certain value of transconductance to be used that leads to low gain, and hence, high NF. Noise-reduction techniques are used to overcome the disadvantage of the CGLNA configuration [12]–[17]. The gain boosting scheme using negative feedback employing capacitive cross-coupling [12], [13], dual negative feedback [16], and positive-negative feedback [17] are applied to break the tradeoff between the input matching condition and the NF, which lead to simultaneous reduction in noise and power dissipation. However, reducing the NF below 2 dB is still challenging in CGLNAs.

In this paper, a wideband differential CGLNA employing multiple feedback is proposed. It uses three feedbacks to add more flexibility in determining the $g_{mn}$ of the impedance matching device. This breaks the lower bound of the noise performance and leads to reduction in the NF and increase in the gain. To the best of the authors’ knowledge, the proposed LNA achieves the lowest NF and highest gain among CGLNAs reported in the literature while consuming low power. It also avoids the use of bulky inductors resulting in considerable area and cost savings. The presented LNA covers frequency bands for digital video broadcasting (DVB) at 450–850 MHz, global...
system for mobile communications (GSM) at 900 MHz, and
global positioning system (GPS) at 1.2 and 1.5 GHz, providing
a practical solution for multistandard applications. This paper
is organized as follows. In Section II, existing noise-reduction
techniques for the CGLNA using negative and positive feedbacks
are discussed. Section III covers the proposed CGLNA,
showing detailed analysis for the major LNA parameters. In
Section IV, circuit implementation is presented along with sim-
ulation results and measurements. Finally, Section V concludes
this paper.

II. BACKGROUND

Fig. 1(a) shows the differential configuration of the conven-
tional CGLNA. In this circuit, the differential voltage gain
$A_v = (V_{op} - V_{on})/(V_{ip} - V_{in})$ and the differential input
impedance $R_{in}$ are given by

$$A_v = g_{m1} R_L$$

$$R_{in} = 2g_{m1}$$

where $g_{m1}$ is the transconductance of transistor $M_1$. Assuming
perfect matching condition ($R_{in} = 2R_S = 100 \Omega$), the noise
factor $F$ is given by

$$F = 1 + \frac{\gamma}{\alpha} + \frac{AR_S}{RL}$$

where $\gamma$ is the excess channel thermal noise coefficient, and
$\alpha$ is the ratio between $g_{m1}$ and the zero-bias drain conduc-
tance, $g_{d01}$. The last term in (3) represents the noise contribu-
tion due to the load, $R_L$. Due to the power matching constraint,
the CGLNA suffers a relatively high NF. Noise-reduction tech-
niques are used to improve the NF of the CGLNA. In the Sec-
tions II-A and II-B, these techniques are briefly presented.

A. Negative Feedback CGLNA Employing Capacitive
Cross-Coupling

The idea to improve the noise performance of the CGLNA
is based on introducing a decoupling mechanism between the
input power matching condition and the NF. This is achieved
by improving the effective transconductance and enhancing the

$A_{NEG}$ by

$$A_{NEG} = \frac{g_{m2} R_L}{g_{m1}}$$

The single-ended model of the transconductance boosting
structure is shown in Fig. 1(b). The structure uses an inverting
gain $A_{NEG}$ that is inserted in the feedback between the gate
and source terminals of $M_1$. The effective $g_{m1}$ is boosted to
$g_{m1}(1 + A_{NEG})$ with input impedance matching of $1/(g_{m1}(1 +
A_{NEG})) = R_S = 50 \Omega$. This means smaller bias current, less
channel noise from $M_1$, and consequently smaller noise contribu-
tion and power consumption. The noise factor $F$ is then given
by

$$F = 1 + \frac{\gamma}{(1 + A_{NEG})\alpha} + \frac{AR_S}{RL}$$

One possible way to implement the inverting gain $A_{NEG}$ is
to use cross-coupling capacitors $C_1$, as shown in the differen-
tial CGLNA topology in Fig. 1(c) [12]. $A_{NEG}$ is approximately
given by the capacitors ratio ($C_1 - C_{psl})/(C_1 + C_{psl})$, where
$C_{psl}$ is the gate–source capacitance of $M_1$. For $C_1 \gg C_{psl},$
$A_{NEG}$ is almost unity, which reduces $A_v$, $R_{in}$, and $F$ to the fol-
lowing:

$$A_v = 2g_{m1}R_L$$

$$R_{in} = 2R_S = 1/g_{m1}$$

$$F = 1 + \frac{\gamma}{2\alpha} + \frac{AR_S}{RL}$$

Comparing to the conventional CGLNA, $F$ is reduced and the
effective transconductance is increased with reduction in power
consumption.

B. Positive–Negative Feedback CGLNA

The negative feedback CGLNA reduces the NF by the use of
capacitive divider. Meanwhile, its transconductance $g_{m1}$ is
restricted to 10 mS to satisfy the input power matching condi-
tion. Thus, this solution suffers from low gain. To alleviate the
restriction of low $g_{m1}$, a positive feedback along with the neg-
ative feedback is used in [17]. To increase the gain, the idea is
to create a positive current feedback path through $M_2$, as
shown in the single-ended model in Fig. 1(d). This feedback
path increases the input impedance of the LNA to be equal to
$1/(g_{m1}(1 + A_{NEG})(1 - A_{POS})$, where $A_{POS} = g_{m2}R_L$ is the
positive feedback gain, which varies from 0 to 1 for stability. In this way, \( g_{m1} \) can be chosen arbitrarily to values higher than 10 mS without restricting the input matching condition. For example, if \( A_{\text{POS}} \) is designed to be 0.5 and \( A_{\text{NEG}} = 1 \), then \( g_{m1} = 20 \) mS for the 50-\( \Omega \) input matching to be satisfied. Thus, the gain increases.

The fully differential positive-negative CGLNA in [17] is shown in Fig. 1(e). Since the positive feedback loop provides a degree of freedom in a way that the impedance matching does not fix the bias current, the current will be a design variable to improve the noise performance. Considering the thermal channel noise, under input matching condition, the noise factor is given by

\[
F = 1 + \frac{(1 - A_{\text{POS}})\gamma}{(1 + A_{\text{NEG}})\alpha} + g_{m2}R_S\frac{\gamma}{\alpha} + \frac{R_S}{R_L}(2 - A_{\text{POS}})^2.
\tag{8}
\]

For \( A_{\text{NEG}} = 1 \) and \( A_{\text{POS}} = 0.5 \), \( A_v \), \( R_{\text{in}} \), and \( F \) are reduced to the following:

\[
A_v = 2g_{m1}R_L,
\tag{9}
\]

\[
R_{\text{in}} = 2R_S = 2/g_{m1}
\tag{10}
\]

\[
F = 1 + \frac{\gamma}{4\alpha} + g_{m2}R_S\frac{\gamma}{\alpha} + \frac{9R_S}{4R_L}.
\tag{11}
\]

The third term in (11) represents the noise due to \( M_2 \). The value of \( g_{m2} \) is chosen to be small, which translates to small noise contribution. Therefore, the positive-negative feedback CGLNA can achieve a lower NF than the negative feedback and conventional CGLNAs with higher gain. However, power consumption increases compared to negative feedback CGLNA.

### III. PROPOSED CGLNA

The idea of the proposed CGLNA is based on adding an additional degree of freedom on the impedance-matching condition of the positive-negative feedback CGLNA in Fig. 1(e). In this way, there will be more flexibility in choosing the optimum value of the LNA transconductance that achieves minimum NF. Fig. 2 shows the proposed CGLNA. The biasing inductors are replaced by current sources \([13]\) that are capacitively cross-coupled using \( C_2 \) (\( C_2 \gg C_{\text{gs}3} \)) [13]. As shown
in the single-ended model in Fig. 3, the capacitively coupled transistor $M_3$ creates another positive current feedback path beside the one created by $M_2$. Therefore, the output current of the LNA becomes the sum of the current provided by the source and those injected through $M_2$ and $M_3$, making the current gain larger than unity.

A. Input Impedance

The two current (shunt) positive feedback paths have the effect of increasing the CGLNA input impedance. Referring to Fig. 2, the input impedance is given by

$$R_{\text{in}} = \frac{2}{g_{m1} (1 + A_{\text{NEG}}) (1 - A_{\text{POS}} - B_{\text{POS}})} = \frac{2}{2g_{m1} (1 - A_{\text{POS}} - B_{\text{POS}})}$$

where $A_{\text{POS}} = g_{m2} R_L$, $B_{\text{POS}} = g_{m3}/2g_{m1}$, and $A_{\text{NEG}} = 1$. Thus, the input matching condition is given by

$$2g_{m1} R_L (1 - A_{\text{POS}} - B_{\text{POS}}) = 1.$$ (13)

From (13), two degrees of freedom, $A_{\text{POS}}$ and $B_{\text{POS}}$, exist that allow arbitrary choice of $g_{m1}$ achieving high gain and optimum minimum NF, as will be seen in the noise analysis.

B. Stability

The condition of stability is based on the approach of the return ratio (RR) [15]. This approach is used to study the amplifier stability in the presence of multiple feedback loops and to model bidirectional paths between input and output. For the proposed CGLNA, the RR has the following expression:

$$\text{RR} = \frac{-2g_{m1} R_L}{1 + 2g_{m1} R_L} (A_{\text{POS}} + B_{\text{POS}}).$$ (14)

The proposed CGLNA is stable if $-1 < \text{RR} < 0$ and this can be guaranteed by setting $(A_{\text{POS}} + B_{\text{POS}}) < 1$ with a safe margin to take into account any process variation.

C. Noise Analysis

Fig. 4 shows a simplified model for the noise sources of the proposed CGLNA. The circuit noise performance is analyzed and its NF is computed assuming that the dominant noise sources are due to the thermal noise of the transistors and the load. The coupling capacitors, $C_1$ and $C_2$, in Fig. 2 are replaced with short circuits since they are much larger than the gate capacitance of the input transistors $M_1$ and $M_3$, respectively. In this case, the noise due to the source resistance

<table>
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<tr>
<th>TABLE I</th>
<th>COMPARISON BETWEEN DIFFERENT CGLNA CONFIGURATIONS TOGETHER WITH THE PROPOSED ONE</th>
</tr>
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<tbody>
<tr>
<td>Differential input impedance, $R_{\text{in}}$</td>
<td>$\frac{g_{m1}}{g_{m1}}$</td>
</tr>
<tr>
<td>$g_{m1}$ for the input matching</td>
<td>$\frac{1}{R_G}$</td>
</tr>
<tr>
<td>$A_{\text{in}}$ at the input matching</td>
<td>$\frac{R_L}{R_G}$</td>
</tr>
<tr>
<td>$NF$ at the input matching</td>
<td>$1 + \frac{1}{\alpha} + \frac{4R_g}{R_L}$</td>
</tr>
<tr>
<td>Percentage of $NF$ reduction relative to the conventional CGLNA</td>
<td>–</td>
</tr>
</tbody>
</table>

Fig. 6. Schematic of the entire LNA with the output buffer.

<table>
<thead>
<tr>
<th>TABLE II</th>
<th>TRANSISTOR ASPECT RATIOS FOR THE LNA AND BUFFER</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W/L$</td>
<td>$M_1$</td>
</tr>
<tr>
<td>0.175</td>
<td>0.12</td>
</tr>
</tbody>
</table>

Fig. 7. Die photograph of the proposed LNA.
Assuming \( \gamma_1 = \gamma_2 = \gamma_3 = \gamma \), the noise factor \( F \) is given by

\[
F = \frac{\overline{\nu}_S^2}{\overline{\nu}_{S\text{-out}}^2} = 1 + \frac{\gamma (g_{m1} R_s - 1)^2}{g_{m1} R_s} + \frac{\gamma}{\alpha} g_{m2} R_s \\
+ \frac{\gamma}{\alpha} g_{m3} R_s + \frac{R_s}{R_L} \left( 1 + \frac{1}{2g_{m1} R_s} \right)^2. \tag{16}
\]

Note that the last term accounts for the noise contribution due to the load \( R_L \). Increasing the value of \( R_L \) relative to \( R_s \) reduces the load noise contribution to the overall NF. Under the input power matching condition, \((2g_{m1} R_s[1 - A_{\text{POS}} - g_{m3}/2g_{m1}] = 1)\ F \) reduces to

\[
F = 1 + \frac{\gamma (\eta - 1)^2}{\eta} + 2 \frac{\gamma}{\alpha} (1 - A_{\text{POS}}) \eta - \frac{\gamma}{\alpha} \left( 1 - \frac{R_s}{R_L} A_{\text{POS}} \right) \\
+ \frac{R_s}{R_L} \left( 1 + \frac{1}{2\eta} \right)^2. \tag{17}
\]

where \( \eta = g_{m1} R_s \) and \( A_{\text{POS}} \) are the optimization parameters used to determine the minimum noise factor for the proposed CGLNA. To find the optimum value of \( \eta, dF/d\eta = 0 \). As a result, for large \( R_L \),

\[
\eta_{\text{opt}} = \frac{1}{\sqrt{3 - 2A_{\text{POS}}}}. \tag{18}
\]
TABLE III

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Gain (dB)</th>
<th>Freq. Range (GHz)</th>
<th>(N_{F_{\text{min}}}) (dB)</th>
<th>(N_{F_{\text{max}}}) (dB)</th>
<th>IIP3 (dBm)</th>
<th>(P_{DC}) (mW)</th>
<th>Area (mm²)</th>
<th>Tech</th>
<th>Topology</th>
</tr>
</thead>
<tbody>
<tr>
<td>[16]</td>
<td>16.9</td>
<td>1.05-3.05</td>
<td>2.57</td>
<td>3.2 (a)</td>
<td>-0.7</td>
<td>12.6</td>
<td>0.073 (c)</td>
<td>0.18</td>
<td>Single-Ended CG</td>
</tr>
<tr>
<td>[17]</td>
<td>21</td>
<td>0.3-0.92</td>
<td>3.5 (c)</td>
<td>3.2 (a)</td>
<td>2.7</td>
<td>32.4</td>
<td>0.12 (c)</td>
<td>0.18</td>
<td>Differential CG</td>
</tr>
<tr>
<td>[18]</td>
<td>20.5 (b)</td>
<td>0.02-1.18</td>
<td>3 (a)</td>
<td>3.5 (a)</td>
<td>2.7</td>
<td>32.4</td>
<td>0.075 (c)</td>
<td>0.12</td>
<td>Differential CG parallel Resistive Feedback</td>
</tr>
<tr>
<td>[19]</td>
<td>13.7</td>
<td>0.002-1.6</td>
<td>1.9 (a)</td>
<td>2.4</td>
<td>0</td>
<td>35</td>
<td>0.075 (c)</td>
<td>0.18</td>
<td>Single-Ended Resistive Feedback parallel CS</td>
</tr>
<tr>
<td>[20]</td>
<td>16</td>
<td>0.1-0.4</td>
<td>3.5</td>
<td>5.3</td>
<td>-17</td>
<td>16.8</td>
<td>0.12 (c)</td>
<td>0.18</td>
<td>Single-Ended Resistive feedback</td>
</tr>
<tr>
<td>[21]</td>
<td>21</td>
<td>0.002-2.3</td>
<td>1.4</td>
<td>1.7</td>
<td>-1.5</td>
<td>18</td>
<td>0.06 (c)</td>
<td>0.18</td>
<td>Differential Resistive feedback</td>
</tr>
<tr>
<td>[22]</td>
<td>12.5 (b)</td>
<td>0.8-2.1</td>
<td>2.5 (a)</td>
<td>2.7 (a)</td>
<td>16</td>
<td>17.4</td>
<td>0.1</td>
<td>0.13</td>
<td>Single-Ended CG and CS cascade</td>
</tr>
<tr>
<td>[23]</td>
<td>18</td>
<td>0.1-1.5</td>
<td>2.5 (a)</td>
<td>4</td>
<td>-8</td>
<td>20</td>
<td>N.A.</td>
<td>0.13</td>
<td>Single-to-Differential Resistive Active Feedback</td>
</tr>
<tr>
<td>[24]</td>
<td>19</td>
<td>0.2-3.8</td>
<td>2.8</td>
<td>3.4</td>
<td>-4.2</td>
<td>5.7</td>
<td>0.025 (c)</td>
<td>0.13</td>
<td>Differential CG parallel CS</td>
</tr>
<tr>
<td>This work</td>
<td>23</td>
<td>0.1-1.77</td>
<td>1.85</td>
<td>2.35</td>
<td>-2.85</td>
<td>2.8</td>
<td>0.03 (c)</td>
<td>0.18</td>
<td>Differential CG</td>
</tr>
</tbody>
</table>

(a) Estimated from data provided in the corresponding papers.
(b) Power gain.
(c) Active area size.

For small values of \(A_{\text{FOS}}\), (18) becomes

\[
\eta_{\text{opt}} = \frac{1}{\sqrt{3}} \left( 1 + \frac{A_{\text{FOS}}}{3} \right). \tag{19}
\]

Accordingly, the minimum noise factor, \(F_{\text{min}}\), is given by

\[
F_{\text{min}} = 1 + 0.461 \frac{\gamma}{\alpha} - \frac{\gamma}{\alpha} \left( 1.155 - \frac{R_s}{R_L} \right) A_{\text{FOS}} + \frac{R_s}{R_L} (1.866 - 0.2886 A_{\text{FOS}})^2. \tag{20}
\]

The negative sign for the third term in (17) plays an important role in reducing the proposed CGLNA noise factor. We can say that the combination of multiple feedbacks contributes to noise cancellation. As an example, for \(A_{\text{FOS}} = 0.35\) to ensure stability, \(F_{\text{min}}\) is given by

\[
F_{\text{min}} = 1 + \left( 0.06 + 0.35 \frac{R_s}{R_L} \right) \frac{\gamma}{\alpha} + 3.11 \frac{R_s}{R_L}. \tag{21}
\]

Graphically, Fig. 5 shows the NF versus sweep of the optimization parameter \(\eta\). As depicted, there is an optimum value \(\eta_{\text{opt}}\) to minimize the NF, which is confirmed by the above analysis. In this design example, a minimum NF, \(N_{F_{\text{min}}}\), of 1.4 dB can be achieved for typical values of short-channel devices. Compared to the conventional CGLNA and other reported feedback-based CGLNA topologies, the proposed CGLNA achieves the lowest NF with advantages of removing the bulk inducers and arbitrary choice of \(g_{m1}\) without restricting the input matching condition. Table I summarizes the main properties of the different CGLNA configurations together with the proposed one. The last line is showing the percentage of reduction in NF for each feedback method relative to the conventional CGLNA at \(R_L = 650 \Omega\). \(\gamma = (4/3)\), and \(\alpha = 0.8\). It can be shown that the proposed CGLNA can achieve the highest reduction among other topologies.

IV. CIRCUIT DESIGN AND MEASUREMENT RESULTS

The proposed LNA with a voltage gain of 23 dB, 3-dB bandwidth of 1.76 GHz, and a minimum NF of 1.85 dB over the band is implemented. A highly linear voltage buffer is used at the LNA output to drive the 50-Ω load of the measuring equipment. Coupling capacitors are used between the LNA and the buffer to provide the buffer with separate dc bias. The gain and NF of the buffer are predetermined to de-embed their effect from the overall response to get the LNA response. The total schematic of the LNA with the buffer is shown in Fig. 6. Table II shows the transistor aspect ratios for the proposed LNA and buffer. In the layout implementation, the transistors are laid out with maximum number of fingers and close to minimum width per finger to minimize the effective series gate resistance to reduce the signal loss and improve the NF specially for the input transistor \(M_1\). To reduce the effect of the flicker noise, the lengths of the transistors are increased. The coupling capacitors, employed in the design, are implemented using a MIMCAP device supported by the IBM 90-nm CMOS process, which has a density of 5.8 fF · μm². The biasing resistors are implemented using poly resistors. Fig. 7 shows a micrograph of the fabricated CGLNA/buffer with a chip size of 1 mm × 1 mm (including the pads). The core LNA area is 0.03 mm².

The core LNA consumes 1.4 mA from a 2-V supply while the buffer consumes 10 mA. The LNA is encapsulated in a micro leadframe (QFN) open package, where the dc biases and input RF signal are applied/monitored using an FR-4 printed circuit board (PCB). The output signal is monitored using a ground–signal–ground–signal–ground (G–S–G–S–G) differential probe. This measurement setup is used to evaluate the performance of the LNA including the PCB traces and packaging effect. Baluns are used at the input and output for single-ended to differential signal conversion. Figs. 8–10 show the post layout simulated and the measured input reflection coefficient \(S_{11}\), voltage gain, and NF, respectively. They are plotted versus RF input frequency up to 2 GHz after de-embedding the effect of the output buffer. The measured \(S_{11}\) is lower than −10 dB from 100 MHz up to 1.8 GHz (Fig. 8). The voltage gain is measured to be 23 dB in the passband with an upper 3-dB frequency of 1.77 GHz (Fig. 9). The measured minimum NF is 1.85 dB at 0.7 GHz with degraded performance at the lower and higher frequencies because of the flicker noise and LNA bandwidth limitation, respectively. Across the entire 3-dB bandwidth, the average measured NF is 2 dB. These measurements show that the proposed LNA achieves an almost constant NF from 100 MHz up to its upper cutoff frequency. This property does not exist in many reported broadband LNAs.
which achieve a minimum NF at a specific frequency and have a much higher NF across the entire frequency range. The input-referred intercept point, $\Pi P_3$, for the proposed wideband CGLNA is measured using a two-tone test for a 300-MHz operating frequency. The two tones are applied with the same amplitude and a frequency offset of 10 MHz. An $\Pi P_3$ value of $-2.85$ dBm is obtained, as shown in Fig. 11. As a measure of the stability of the proposed CGLNA, Fig. 12 shows a plot for the stability factor $K$ that is calculated based on the $S$-parameters (LNA + buffer) through the following expression:

$$K = \frac{1 - |S_{11}|^2 - |S_{21}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}|^2|S_{21}|}.$$  \[(22)\]

Table III compares the performance of the proposed CGLNA with that of the state-of-the-art wideband LNAs around the same frequency range. The power consumption reported is of the core LNA only. As shown in this table, the proposed broadband LNA with multiple feedback provides the minimum NF among common-gate (CG) topologies. It also has low power consumption and high gain when compared to previously reported wideband LNAs.

V. CONCLUSION

An inductorless broadband CGLNA employing noise reduction has been proposed in this paper. The LNA relies on multiple feedbacks to fully decouple the tradeoff between noise and input power matching. The theory shows that the proposed approach reduces the lower limit of the noise performance of the previously reported CGLNAs, allowing for an NF around 1.4 dB. Measurements of a fabricated prototype in 90-nm CMOS technology show a voltage gain of 23 dB with a 3-dB bandwidth of 1.77 GHz. A minimum NF of 1.85 dB and an $\Pi P_3$ of $-2.85$ dBm are also measured. The measured NF is lower than the best reported NF of CGLNAs. The LNA consumes 2.8 mW from a 2-V supply.

REFERENCES


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