ECEN 326 LAB 5
Design of a MOS Differential Amplifier

1 Circuit Topology

The following figure shows a typical MOS differential amplifier. Assume \( k_n' = 100 \mu A/V^2 \), \( V_{tn} = 1.4 V \), \( \lambda_n = 0.01 V^{-1} \), \( W = 6 \mu m \), and \( L = 1 \mu m \) for all NMOS transistors.

The tail current source \((I_T)\) can be calculated from

\[
V_{SS} = I_{D4}R_B + V_{GS4}
\]
\[
I_{D4} = \frac{k_n' W}{2L} (V_{GS4} - V_{tn})^2
\]
\[
I_T = I_{D3} = I_{D4}
\]

DC drain currents of \( M_1 \) and \( M_2 \) are

\[
I_{D1} = I_{D2} = \frac{I_T}{2}
\]

Assuming \( r_{o1}, r_{o2} \gg R_D \), small-signal differential-mode gain can be obtained as

\[
A_{dm} = \frac{v_{od}}{v_{id}} \approx -\frac{R_D}{g_{m1}} = -g_{m1}R_D
\]

where \( g_{m1} = \sqrt{2k_n' W/I_{D1}} \). Common-mode gain can be found as

\[
A_{cm} = \frac{v_{oc}}{v_{ic}} \approx -\frac{R_D}{g_{m1}} + 2R_T
\]

where \( R_T = r_{o3} = \frac{1}{\lambda_n I_{D3}} \). Common-mode rejection ratio (CMRR) can be calculated from

\[
CMRR = 20 \log \left| \frac{A_{dm}}{A_{cm}} \right|
\]
2 Pre-Lab

Design a MOS differential amplifier with the following specifications:

\[
\begin{array}{|c|c|}
\hline
V_{ic} = 0 \text{ V} & I_{supply} \leq 0.5 \text{ mA} \\
V_{DD} = V_{SS} = 5 \text{ V} & \text{THD} \leq 5\% \text{ for } V_{od} = 5 \text{ V zero-to-peak @ 1 kHz} \\
|A_{dm}| \geq 10 \\
\hline
\end{array}
\]

1. Show all your calculations, design procedure, and final component values.

2. Simulate your circuit using N4007 transistor models in PSPICE. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.

3. Using PSPICE, perform Fourier analysis and show that the total harmonic distortion (THD) is less than 5% when the differential output voltage \( V_{od} \) is 5 V zero-to-peak at 1 kHz. Submit transient and Fourier plots for \( V_{od} \), and the distortion data from the output file.

4. Be prepared to discuss your design at the beginning of the lab period with your TA.

3 Lab Procedure

1. Construct the amplifier you designed in the pre-lab.

2. Connect \( V_{i1} \) and \( V_{i2} \) to ground and record all DC quiescent voltages and currents. If any DC bias value (especially \( I_D \)) is significantly different than the one obtained from Pspice simulations, modify your circuit to get the desired DC bias before you move onto the next step.

3. Measure \( I_{supply} \) and the output offset voltage \( V_{o1} - V_{o2} \).

4. Using a 1:1 center-tapped transformer, apply differential input signals at 1 kHz to the amplifier as shown below, and measure \( A_{dm} \).

5. Adjust the input signal level so that the differential output voltage is 5 V zero-to-peak. Measure the THD at the differential output.

6. Disconnect the transformer and connect both inputs to the signal generator. Measure \( A_{cm} \) and calculate CMRR.

7. Prepare a data sheet showing your simulated and measured values.

8. Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.