1 Circuit Topology and Design Equations

The following figure shows a typical BJT differential amplifier. Assume \( \beta \geq 100 \) and \( V_A = 75 \text{ V} \).

The tail current source \( (I_T) \) can be calculated from

\[
I_T \approx \frac{R_{B2}}{R_{B1} + R_{B2}} V_{EE} - 0.7
\]

provided that \( I_{B3} \ll I_{R_{B2}} \). DC collector currents of \( Q_1 \) and \( Q_2 \) are

\[
I_{C1} = I_{C2} \approx \frac{I_T}{2}
\]

Assuming \( r_{o1}, r_{o2} \gg R_C, R_E \), small-signal differential-mode gain can be obtained as

\[
A_{dm} = \frac{v_{od}}{v_{id}} \approx -\frac{R_C}{r_{e1} + R_E}
\]

where \( r_{e1} \approx V_T/I_{C1} \). Common-mode gain can be found as

\[
A_{cm} = \frac{v_{oc}}{v_{ic}} \approx -\frac{R_C}{r_{e1} + R_E + 2R_T}
\]

where

\[
R_T = r_{o3} + R_{BB} + g_{m3} \frac{r_{\pi3}}{r_{\pi3} + (R_{B1} \parallel R_{B2})} r_{o3} R_{BB}
\]

\[
R_{BB} = R_{B3} \parallel (r_{\pi3} + (R_{B1} \parallel R_{B2}))
\]

Common-mode rejection ratio (CMRR), differential-mode input resistance \( (R_{id}) \) and common-mode input resistance \( (R_{ic}) \) are given by

\[
CMRR = 20 \log \frac{|A_{dm}|}{|A_{cm}|}
\]

\[
R_{id} \approx 2(\beta + 1)(R_E + r_{e1})
\]

\[
R_{ic} \approx (\beta + 1)(2R_T \parallel r_{o1})
\]
Because of mismatches between the transistors and load resistors, a non-zero differential output voltage will result when the differential input voltage is zero. We may refer this output offset voltage back to the input as

\[ V_{OS} = \frac{V_o}{A_{dm}} \]

\( V_{OS} \) is known as the input-referred offset voltage. Since the two sources of the offset voltage are uncorrelated, it can be estimated as

\[ V_{OS} = V_T \sqrt{\left(\frac{\Delta R_C}{R_C}\right)^2 + \left(\frac{\Delta I_S}{I_S}\right)^2} \]

2 Pre-Lab

Design a BJT differential amplifier with the following specifications:

- \( V_{ic} = 0 \) V
- \( I_{supply} \leq \) 3 mA
- Zero-to-peak un-clipped swing at \( V_{o1} \geq 2.5 \) V
- \( V_{cc} = V_{ee} = 5 \) V
- \( |A_{dm}| = 40 \)
- Operating frequency: 1 kHz
- \( R_{id} \geq 20 \) kΩ
- CMRR \( \geq 70 \) dB

1. Show all your calculations and final component values.
2. Verify your results using PSpice. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
3. Using PSpice, perform Fourier analysis and determine the differential input and output signal amplitudes resulting in 1% and 5% total harmonic distortion (THD) at the differential output. Submit transient and Fourier plots, and the distortion data from the output file for both cases.
4. Be prepared to discuss your design at the beginning of the lab period with your TA.

3 Lab Procedure

1. Construct the amplifier you designed in the pre-lab.
2. Connect \( V_{i1} \) and \( V_{i2} \) to ground and record all DC quiescent voltages and currents.
3. Measure \( I_{supply} \) and the output offset voltage \( V_{o1} - V_{o2} \).
4. Using a 1:1 center-tapped transformer, apply differential input signals to the amplifier as shown below:

5. Measure the maximum un-clipped output signal amplitude at \( V_{o1} \).
6. Measure \( A_{dm} \) and \( R_{id} \).
7. Apply the input signal levels resulting in 1% and 5% THD at the differential output voltage, and measure the input and output signal amplitudes.
8. Disconnect the transformer and connect both inputs to the signal generator. Measure \( A_{cm} \) and calculate CMRR.
9. Prepare a data sheet showing your simulated and measured values.
10. Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.