1. The ac schematic of a shunt-shunt feedback amplifier is shown below. All transistors have $I_D = 1$ mA, $(W/L) = 100$, $k'_n = 60 \mu A/V^2$, and $\lambda_n = (1/50) V^{-1}$.

(a) Calculate the overall gain $v_o/i_i$, the loop gain, the input and output impedance at low frequencies.

(b) If the circuit is fed from a source resistance of $1 \, \text{k} \Omega$ in parallel with $i_i$, what is the new output resistance of the circuit?

2. For the below feedback amplifier, $\beta_{npn} = 200$, $\beta_{pnp} = 100$, $|V_{BE(on)}| = 0.7$ V, and $|V_A| = \infty$, If the dc input voltage is zero, calculate the overall gain $v_o/v_i$, the loop gain, and the input/output impedance at low frequencies. Compare your answers with PSPICE. Use PSPICE to plot the complete large-signal transfer function $v_o$ vs. $v_i$, and find the second and third harmonic distortions in $v_o$ for a sinusoidal input voltage with 0.5Vpp at $v_i$. 
3. A commercial wideband monolithic feedback amplifier (the 733) is shown below. This consists of a local series-feedback stage feeding a two-stage shunt-shunt feedback amplifier. Assume \( \beta = 100, |V_{BE(on)}|=0.7\text{V}, \text{ and } |V_A| = \infty, \)

(a) Calculate the collector bias current of in each device
(b) Calculate input/output impedance, and the overall gain \((v_o/v_i)\) of the circuit at low frequencies for \(R_L=2\ \text{k}\Omega\). Calculate the loop gain of the second stage. Compare your answers with PSPICE.

![ Circuit Diagram](image)

4. A variable-gain CMOS amplifier is shown below. Note that M4 represents the shunt feedback around M6. Assuming that the bias voltage of \(V_i\) is adjusted so that \(V_{GD6}=0\ \text{V dc}\), calculate bias currents in all devices and the small signal voltage gain and output resistance for \(V_c=3\) and then 4 V. Assume \( k'n = 60 \ \mu\text{A/V}^2, k'p=30 \ \mu\text{A/V}^2, V_{tn}=|V_{tp}|=0.8, \lambda_n =\lambda_p=0. \)

![ Circuit Diagram](image)